US-PAT-NO: 7094669

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TITLE: Structure and method of liner air gap formation

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Abstract Text - ABTX (1):

A structure and method of a semiconductor device with liner air gaps next to interconnects and **dielectric** layers. A **dielectric** layer is formed over a lower **dielectric** layer and a lower interconnect over a substrate. We form an interconnect opening in the **dielectric** layer. The opening has sidewalls of the **dielectric** layer. A sacrificial liner is formed over the sidewalls of the interconnect opening. An upper interconnect is formed that fills the opening. We remove the sacrificial liner/spacers to form (air) liner gaps.

Application Filing Date - AD (1):
20040803

Brief Summary Text - BSTX (3):

The embodiments of the invention relates generally to fabrication of semiconductor devices and relates to air-gap-containing metal/**insulator** interconnect structures for Very Large Scale Integrated (VLSI) and Ultra Large Scale Integrated (ULSI)semiconductor devices and packaging, and more particularly to structures, methods, and materials relating to the incorporation of voids, cavities or air gaps into multiple levels of multilayer interconnect structures for reducing wiring capacitance.

Brief Summary Text - BSTX (5):

Copper interconnects are formed using a dual damascene process. The incorporation of low-k **insulator** material may be accomplished by depositing an etch stop layer and a first layer of low-k **dielectric** material over a copper interconnect. This may be followed by an optional etch stop barrier **insulator** and then a second layer of low-k material. A via is then etched through the second layer of low-k material, any etch stop barrier **insulator,** and the first layer of low-k **dielectric** material to reach the copper interconnect. A trench is then etched into the second layer of low-k material to aid in forming another layer of copper interconnects. Barrier metal and copper are deposited

by sputtering, chemical vapor deposition (CVD), electrochemical deposition, or a combination of these methods. The deposited copper, and possibly the barrier metal, will then be planarized using chemical mechanical polishing (CMP) to form copper interconnects.

Brief Summary Text - BSTX (6):

Air gaps have been used for intra-level **insulators** for copper, while using silicon oxide or low-k at the inter-level **dielectric** layers. The air gaps are formed by decomposing sacrificial polymer. However, prior art air gaps can be improved.

Brief Summary Text - BSTX (8):

US 20020158337 A1--Babich, et al.--Multilayer interconnect structure containing air gaps and method for making--an air-gap-containing interconnect wiring structure is described incorporating a solid low-k **dielectric** in the via levels, and a composite solid plus air-gap **dielectric** in the wiring levels.

Brief Summary Text - BSTX (11):

U.S. Pat. No. 6,495,906 Smith, et al.--Simplified process for producing nanoporous silica--relates to low **dielectric** constant nanoporous silica films and to processes for their manufacture. A substrate, e.g., a wafer suitable for the production of an integrated circuit, having a plurality of raised lines and/or electronic elements present on its surface, is provided with a relatively high porosity, low **dielectric** constant, silicon-containing polymer film composition.

Brief Summary Text - BSTX (12):

U.S. Pat. No. 6,670,022 Wallace, et al.--Nanoporous **dielectric** films with graded density and process for making such films--relates to nanoporous **dielectric** films and to a process for their manufacture. A substrate having a plurality of raised lines on its surface is provided with a relatively high porosity, low **dielectric** constant, silicon containing polymer composition positioned between the raised lines and a relatively low porosity, high **dielectric** constant, silicon containing composition positioned on the lines.

Brief Summary Text - BSTX (13):

U.S. Pat. No. 6,423,630 Catabay, et al.--Process for forming low K **dielectric** material between metal lines--A process is disclosed for forming low k **dielectric** material between and over a plurality of spaced apart metal lines previously formed over a **dielectric** layer of an integrated circuit structure.

Brief Summary Text - BSTX (15):

U.S. Pat. No. 6,342,722 Armacost, et al.--Integrated circuit having air gaps between **dielectric** and conducting lines.

Brief Summary Text - BSTX (16):
U.S. Pat. No. 6,423,629--Ahn, et al.--Multilevel copper interconnects with low-k **dielectrics** and air gaps.

Brief Summary Text - BSTX (18):
The embodiments of the present invention provides a structure and method of a semiconductor device with liner air gaps next to interconnects and **dielectric** layers.

Brief Summary Text - BSTX (19):
An example method embodiment comprises forming a **dielectric** layer over a lower **dielectric** layer and a lower interconnect over a substrate. We form an interconnect opening in the **dielectric** layer. The opening has sidewalls of the **dielectric** layer. A sacrificial liner is formed over the sidewalls of the interconnect opening. An upper interconnect is formed that fills the opening. At some point in the process, we remove the sacrificial spacers to form air liner gaps.

Description Paragraph - DETX (9):
Embodiments show an integration scheme to form liner air gaps adjacent to and/or surrounding metal lines and vias. The presence of liner air gaps can significantly reduce the effective intra-metal **dielectric** constant.

Description Paragraph - DETX (13):
Referring to FIG. 1A, we form an interlevel **dielectric** layer 20 over a substrate 10.

Description Paragraph - DETX (15):
The interlevel **dielectric** (ILD) layer is preferably formed of an low K material, oxide or other **dielectric** material.

Description Paragraph - DETX (19):
We then form an interlevel **dielectric** cap layer 26 over the interlevel **dielectric** layer 20. The cap layer is preferably comprised of SiN or SiC. The cap layer preferably has thickness between 200 and 1000 .ANG.. A purpose of the cap layer is to act as an etch stop and Cu diffusion barrier.

Description Paragraph - DETX (21):
We form an inter metal **dielectric** 1 (IMD1) layer 30 over the ILD cap layer

26. The inter metal **dielectric** layer laterally separates interconnects on the same level. The inter metal **dielectric** is not a liner layer. The inter level **dielectric** layer is preferably comprised of a low k material such as SilK.TM. or Coral.TM. or MSQ or other low-k materials. The inter metal **dielectric** preferably has a thickness between 2000 and 5000 .ANG..

Description Paragraph - DETX (37):
Form a **Dielectric** Layer

Description Paragraph - DETX (38):
Subsequently, we form a (e.g., IMD2) **dielectric** layer 54 over the IMD1 cap layer 50 and IMD1 layer 30. The inter metal **dielectric** is preferably comprised of a low K material (K<3) carbon-doped siloxanes (OSGs), such as Silk.TM. from Dow Chemical (Midland, Mich.), or Coral.TM. Novellus and preferably has a thickness between 4000 and 10,000 .ANG..

Description Paragraph - DETX (39):
Form an Opening in the IMD2 **Dielectric** Layer

Description Paragraph - DETX (40):
As shown in FIG. 1G, we form an interconnect opening 56 in the IMD2 **dielectric** layer 54 to expose the IMD1 cap layer 50.

Description Paragraph - DETX (44):
The sacrificial liner is distinct from a IMD or ILD layer. The sacrificial differs from the inter metal **dielectric** (IMD) layer at least because the sacrificial liner has a property that allows the liner to be removed or decomposed in a subsequent step. Also optionally, the sacrificial liner substantially smaller horizontal width than the IMD or ILD layer. Liner layer typically follow the shape of the interconnect or the interconnect opening in the **dielectric** layer. Interconnect openings are typically formed in the ILD and IMD layer, not in the liner layers. Compared to liner layers, IMD layers or air gaps typically occupy a majority of the horizontal space between interconnects on a level.

Description Paragraph - DETX (58):
In a third option, (selective sac layer depo) referring to FIGS. 3A and 3B and 3C, the sacrificial liner 361 is formed by (a) etching the cap layer 350 to expose the first (level) interconnect 44. Then we (b) form a sacrificial layer 361 using a selective deposition over the cap layer 350 and the IMD2 **dielectric** layer 354, but not on the first (level) interconnect 44.

Description Paragraph - DETX (59):
For example, referring to FIG. 3A, we form the sacrificial layer 361 over the **dielectric** layer(s) (not over the conductive interconnect 44) using a selective deposition process.

Description Paragraph - DETX (62):
A cap layer 80 and **dielectric** layer 84 are formed thereover.

Description Paragraph - DETX (68):
The sacrificial liner can be comprised of carbon which preferably requires oxidation at 450 C. For examples of carbon materials, see Anand, et al., Use of gas as low-k interlayer **dielectric** in LSI's : Demonstration of feasibility, IEEE transactions on electron device, Vol. 44, no. 11, November 1997, pp. 1965 to 1971.

Description Paragraph - DETX (85):
Referring to FIG. 1L, another level of interconnect with spacer gaps 90 92 are formed. FIG. 1L shows a cap layer 80, liner 86, interconnect 94, spacer gaps 92 90, **dielectric** layer 84 and cap layer 98. The spacer gaps 92 90 can be formed using any of the options described above.

Description Paragraph - DETX (87):
The sacrificial liner is distinct from a IMD or ILD layer. The sacrificial differs from the inter metal **dielectric** (IMD) layer at least because the sacrificial layer can be removed or decomposed selectively with respect to the ILD and IMD layers. Also optionally, the sacrificial liner has a substantially smaller horizontal width than the ILD and IMD layers. Liner layer typically follow the shape of the interconnect opening in the **dielectric** layer. Interconnect opens are typically formed in the ILD and IMD layer, not in the liner layers. IMD layers typically occupy a majority of the horizontal spacer between interconnect on a level.

Description Paragraph - DETX (88):
The embodiment's sacrificial liner layer typically has a thickness between 100 and 1000 .ANG.. This contrasts with the inter metal **dielectric** layer (minimum design rule) horizontal thickness that can range between 0.06 and 0.35 .mu.. For example in a 0.13 .mu.m ground rule product, the sacrificial liner would preferably have a horizontal thickness between 100 and 800 .ANG.. In a 0.13 .mu.m ground rule product, the minimum distance between interconnect would between about 0.18 and 0.22 .mu.m. The inter metal **dielectric** layer would fill substantially all the horizontal distance between the interconnects. The interconnect typically has a horizontal width between 0.01 and 0.2 .mu.m. The

line air gap ratio can be 100% in the minimum design rule, but between 0 and 100% in other areas.

Description Paragraph - DETX (91):
The intra-metal **dielectric** constant and the reliability performance can be balanced by running the liner air gap proportion in IMD or by choosing different IMD materials with different E values and mechanical properties.

Description Paragraph - DETX (93):
The advantages of some of the example embodiments include some of the following advantages: Liner air gaps can effectively reduce the intra-metal **dielectric** constant, and hence RC delay and cross-talk etc. The liner air gap structure should have much better reliability performance compared to complete air gap structure. With **dielectric** support, higher level metal structure can be built.

Description Paragraph - DETX (96):
Although this invention has been described relative to specific **insulating** materials, conductive materials and apparatuses for depositing and etching these materials, it is not limited to the specific materials or apparatuses but only to their specific characteristics, such as conformal and nonconformal, and capabilities, such as depositing and etching, and other materials and apparatus can be substituted as is well understood by those skilled in the microelectronics arts after appreciating the present invention

Claims Text - CLTX (1):
1. A method of fabrication of liner gap in a semiconductor device; comprising the steps of: a) forming a **dielectric** layer over a substrate; then b) forming an opening in said **dielectric** layer; said opening has sidewalls of said **dielectric** layer; then c) forming a sacrificial liner over the sidewalls of said opening; then d) forming an upper interconnect filling said opening; and then e) removing said sacrificial liner to form air liner gaps.

Claims Text - CLTX (2):
2. The method of claim 1 wherein before the step of removing said sacrificial liner, which further includes forming a cap layer over said upper interconnect and said **dielectric** layer.

Claims Text - CLTX (6):
6. The method of claim 1 which further includes before step (a): forming a lower **dielectric** layer and a lower interconnect over said substrate; forming a lower cap layer on said lower **dielectric** layer; and said opening is formed by

etching said **dielectric** layer and said lower cap layer to expose said lower interconnect, and forming a sacrificial layer over said opening, and anisotropically etching said sacrificial layer and said lower cap layer to form sacrificial liners on the sidewalls of said opening and exposing said lower interconnect.

Claims Text - CLTX (7):

7. The method of claim 1 wherein said sacrificial liner is formed by forming a sacrificial layer using a selective deposition over said **dielectric** layer.

Claims Text - CLTX (15):

15. A method of fabrication of liner gap in a semiconductor device; comprising the steps of: a) forming a first IMD layer over a structure; then b) forming a trench through said first IMD layer to expose the top surface of said structure; said trench having sidewalls on said first IMD layer; then c) forming a first sacrificial liner over at least the sidewalls of said wench; then d) forming a first interconnect filling said trench; then e) forming a first IMD cap layer over said first interconnect; then f) forming a second IMD **dielectric** layer over said first IMD cap layer and first IMD layer; then g) forming an **opening** in said second IMD **dielectric** layer to expose said first IMD **cap** layer; then h) forming a sacrificial liner over the sidewalls of said opening; then i) forming a second interconnect filling said opening; then j) forming a second IMD cap layer over said second interconnect and said second IMD layer; k) forming a third IMD layer over said second IMD cap layer; l) removing said sacrificial liner to form **air liner gaps**.

Claims Text - CLTX (21):

21. A method of fabrication of liner gap in a semiconductor device; comprising the steps of: a) forming a first IMD layer over a structure: then b) forming a trench through said first IMD layer to expose the surface of said structure; said trench having sidewalls on said first IMD layer; then c) forming a insacrificial liner over at least the sidewalls of said trench; then d) forming a first interconnect filling said trench; then e) forming a first IMD cap layer over said first level interconnect; then f) forming a second IMD layer over said first IMD cap layer and first IMD layer; then g) forming an **opening** in said second IMD **dielectric** layer to expose said first IMD **cap** layer; then h) forming a sacrificial liner over the sidewalls of said opening; then i) forming a second level interconnect filling said opening; 1) said second level interconnect comprised of a metal liner and a metal second level interconnect; then j) forming a second IMD cap layer over said second level interconnect and said second IMD layer; then k) forming a third IMD layer over

said second IMD cap layer; then l) removing sacrificial liner to form **air liner gaps**; and removing said first sacrificial liner spaced to form **air trench liner gaps**.

Claims Text - CLTX (25):

25. The method of claim 21 wherein said sacrificial liner is formed by (a) etching said first IMD cap layer to expose said first interconnect, (b) forming a sacrificial layer using a selective deposition over the sidewalls of said first IMD cap layer and said second IMD **dielectric** layer, but not on said first interconnect.

Other Reference Publication - OREF (1):

Anand, et al., Use of gas as low-k interlayer **dielectric** in LSI's : Demonstration of feasibility, IEEE transactions on electron device, vol. 44, No. 11, Nov. 1997, pp. 1965 to 1971. cited by other

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2475	((trench or opening or hole or via or aperture or groove) with cap$4) and sacrificial and (dielectric or insulating or insulative or insulator)	US-PGPUB; USPAT	OR	ON	2007/06/12 15:02
L2	1548	1 and ((remove or etching or etch or removing) with sacrificial)	US-PGPUB; USPAT	OR	ON	2007/06/12 14:02
L3	683	1 and ((remove or etching or etch or removing) with portion with sacrificial)	US-PGPUB; USPAT	OR	ON	2007/06/12 14:02
L4	434	3 and @ad<"20040916"	US-PGPUB; USPAT	OR	ON	2007/06/12 15:13
L6	2960	((trench or opening or hole or via or aperture or groove) with cap$4) and (air near3 gap) and (dielectric or insulating or insulative or insulator)	US-PGPUB; USPAT	OR	ON	2007/06/12 15:13
L7	2476	6 and @ad<"20040916"	US-PGPUB; USPAT	OR	ON	2007/06/12 15:14
L8	272	(((trench or opening or hole or via or aperture or groove) with cap$4) same (air near3 gap)) and (dielectric or insulating or insulative or insulator)	US-PGPUB; USPAT	OR	ON	2007/06/12 16:11
L9	232	8 and @ad<"20040916"	US-PGPUB; USPAT	OR	ON	2007/06/12 17:07
L10	23	(((trench or opening or hole or via or aperture or groove) with cap$4) same (air near3 pocket)) and (dielectric or insulating or insulative or insulator)	US-PGPUB; USPAT	OR	ON	2007/06/12 16:12
L11	18	10 and @ad<"20040916"	US-PGPUB; USPAT	OR	ON	2007/06/12 15:20
L12	16	(((trench or opening or hole or via or aperture or groove) with cap$4) same (air near3 bridge)) and (dielectric or insulating or insulative or insulator)	US-PGPUB; USPAT	OR	ON	2007/06/12 16:13
L13	15	12 and @ad<"20040916"	US-PGPUB; USPAT	OR	ON	2007/06/12 15:22
L14	5	(((trench or opening or hole or via or aperture or groove) with cap$4) same (air near3 envelope)) and (dielectric or insulating or insulative or insulator)	US-PGPUB; USPAT	OR	ON	2007/06/12 15:22
L15	4	14 and @ad<"20040916"	US-PGPUB; USPAT	OR	ON	2007/06/12 17:09

EAST Search History

L16	747	438/411,421,422,619.ccls. and @ad<"20040916"	US-PGPUB; USPAT	OR	ON	2007/06/12 16:13
L17	445	16 and air	US-PGPUB; USPAT	OR	ON	2007/06/12 15:23
L18	314	16 and (air with (gaps or pocket or bridge or envelope))	US-PGPUB; USPAT	OR	ON	2007/06/12 16:48
L19	386	(((trench or opening or hole or via or aperture or groove) with cap$4) same (air near3 gap)) and (dielectric or insulating or insulative or insulator)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/06/12 16:11
L20	66	(((trench or opening or hole or via or aperture or groove) with cap$4) same (air near3 pocket)) and (dielectric or insulating or insulative or insulator)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/06/12 16:12
L21	6	(((trench or opening or hole or via or aperture or groove) with cap$4) same (air near3 bridge)) and (dielectric or insulating or insulative or insulator)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/06/12 16:13
L22	2144	257/374,501,506,510,522.ccls. and @ad<"20040916"	US-PGPUB; USPAT	OR	ON	2007/06/12 16:48
L23	175	22 and (air with (gaps or pocket or bridge or envelope))	US-PGPUB; USPAT	OR	ON	2007/06/12 17:09
L24	129	23 not 18	US-PGPUB; USPAT	OR	ON	2007/06/12 16:49
L25	356	(brent with a with anderson) or (andres with bryant) or (jeffery with p with gambino) or (anthony with k with stamper)	US-PGPUB; USPAT	OR	ON	2007/06/12 17:10
L26	260	25 and @ad<"20040916"	US-PGPUB; USPAT	OR	ON	2007/06/12 17:09
L27	9	26 and (air with (gaps or pocket or bridge or envelope))	US-PGPUB; USPAT	OR	ON	2007/06/12 17:10
L28	33	(brent with a with anderson) or (andres with bryant) or (jeffery with p with gambino) or (anthony with k with stamper)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/06/12 17:10
L29	0	28 and (air with (gaps or pocket or bridge or envelope))	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/06/12 17:10